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ELECTRONICS ENGINEERING

CONVENTIONAL Practice Sets

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ADVANCED ELECTRONICS

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1 CHAPTER Introduction to VLSI Technology

Q.1 Compare the merits and demerits of CMOS integrated circuits vis-a-vis those of bipolar integrated circuit.

Solution:

	CMOS integrated circuit		Bipolar integrated circuit
1.	Power consumption is very low.	1.	Power consumption is relatively high.
2.	Packing density is very high.	2.	Packing density is comparatively low.
3.	Speed of operation is low compare to bipolar integrated circuit	3.	Speed of operation is relatively high.
4.	Noise margin is very high.	4.	Noise margin is high in one case in other case it is lower than that of CMOS integrated circuit.
5.	Fan out is very high.	5.	Fan out is relatively low.
6.	Frequency of operation is comparatively lower than that of bipolar integrated circuits.	6.	Frequency of operation can be high.
7.	Offers high input impedance, is excellent for constructing simple, low power logic gates.	7.	Input impedance is low therefore power consumption is relatively higher.

Q.2 Why do we use silicon in IC fabrication?

Solution:

- The fabrication of semiconductor devices has been based on the use of silicon as the premier semiconductor. Two other semiconductors, germanium (Ge) and gallium arsenide (GaAs), present special problems while silicon has certain specific advantages not available with the others.
- At 300°K silicon has a band gap of 1.12 eV, while germanium's band gap is 0.66 eV. Because of this small band gap, the intrinsic carrier density of germanium at $T = 300$°K is about 2.5×10^{13}cm^{-3}. At temperatures of about 400°K, this density becomes 10^{15}cm^{-3}, which is comparable to the lower range of doping densities used. This property limits its use to low temperature applications at less than 350°K.
- The other semiconductor of major interest is gallium arsenide. In spite of its attractive electrical properties, gallium arsenide crystals have a high density of crystal defects, which limits the performance of devices made from it.
- Silicon is an abundant element and occurs naturally in the form of sand. It can be refined using simple purification and crystal growth techniques. It also exhibits suitable physical properties for fabricating active devices with good electrical characteristics. In addition silicon can be easily oxidized to form an excellent insulator, (SiO_2) or glass.
- This native oxide is useful, for constructing capacitors and MOSFET's. It also serves as a diffusion barrier that masks against unwanted impurities from diffusing into the high purity silicon material. This masking property allows selective alternation of electrical properties in the silicon.

Q.3 How is electronic grade silicon crystal is obtained?

Solution:

Silicon is the most important semiconductor material used in electronic industry. It is found abundantly in nature in the form of silica and silicate (sand). The main raw material for growth of single silicon crystal is Electronic Grade Silicon (EGS), which is a polycrystalline material of high purity. The major impurities in EGS are boron, carbon and residual donors. To produce EGS, first Metallurgical Grade Silicon (MGS) is produced in a submerged-electrode arc furnace, which is charged with quartzite and carbon. Quartzite is relatively a pure form of sand (SiO_2). The overall reaction for producing MGS is

$$\text{SiC (solid)} + \text{SiO}_2\text{ (solid)} \rightarrow \text{Si (liquid)} + \text{SiO (gas)} + \text{CO (gas)}$$

The drawn MGS is solidified at a purity of 98%. The next step is to crush the silicon and then react it with anhydrous hydrogen chloride to form trichlorsilane ($SiHCl_3$). The reaction is

$$\text{Si (solid)} + \text{3HCl (gas)} \rightarrow \text{SiHCl}_3\text{ (gas)} + \text{H}_2\text{ (gas)} + \text{heat}$$

The reaction takes place in a fluidized bed at a temperature of 300°C to produce trichlorsilane in the presence of catalyst. Trichlorsilane is liquid at room temperature and it has many unwanted chlorides which can be removed by fractional distillation.

The EGS is prepared from purified $SiHCl_3$ in a chemical vapour deposition (CVD) process. The chemical reaction for EGS production is

$$2\text{SiHCl}_3\text{ (gas)} + 2\text{H}_2\text{ (gas)} \rightarrow 2\text{Si (solid)} + 6\text{HCl (gas)}$$

This reaction is also called **hydrogen reduction process.** An alternative method for producing EGS is pyrolysis of silane, which has lower production cost and less harmful reaction by-products. In this process, CVD reactor is operated at 900°C and supplied with silane instead of trichlorsilane. The pyrolysis reaction is

$$\text{SiH}_4\text{ (gas)} + \text{Heat} \rightarrow \text{Si (solid)} + 2\text{H}_2\text{ (gas)}$$

The EGS is in pure form of silicon but in the polycrystalline form. This polycrystalline silicon cannot be used for wafer manufacture. The next step is to grow a single silicon crystal which is usually done via the Czochralski (pronounced "Cha-krawl-ski") method.

Q.4 **If a silicon dioxide (SiO_2) layer of thickness 100 nm is grown by thermal oxidation, what is the thickness of silicon (Si) being consumed? Derive the relation used. The molecular weight of Si is 28.1 g/mol, and the density of Si is 2.33 g/cm^3. The corresponding values for SiO_2 are 60.08 g/mol and 2.21 g/cm^3.**

Solution:

The volume of 1 mol of silicon is,

$$\frac{\text{Molecular weight of Si}}{\text{Density of Si}} = \frac{28.1\text{ g/mol}}{2.33\text{ g/cm}^3} = 12.06\text{ cm}^3\text{/mol}$$

The volume of 1 mol of silicon dioxide is,

$$\frac{\text{Molecular weight of SiO}_2}{\text{Density of SiO}_2} = \frac{60.08\text{ g/mol}}{2.21\text{ g/cm}^3} = 27.18\text{ cm}^3\text{/mol}$$

Since 1 mol of silicon is converted to 1 mol of silicon dioxide,

$$\frac{\text{Thickness of Si} \times \text{area}}{\text{Thickness of SiO}_2 \times \text{area}} = \frac{\text{Volume of 1 mol of Si}}{\text{Volume of 1 mol of SiO}_2}$$

$$\frac{\text{Thickness of Si}}{\text{Thickness of SiO}_2} = \frac{12.06}{27.18} = 0.44$$

$$\text{Thickness of Si} = (0.44)\,(\text{Thickness of SiO}_2)$$

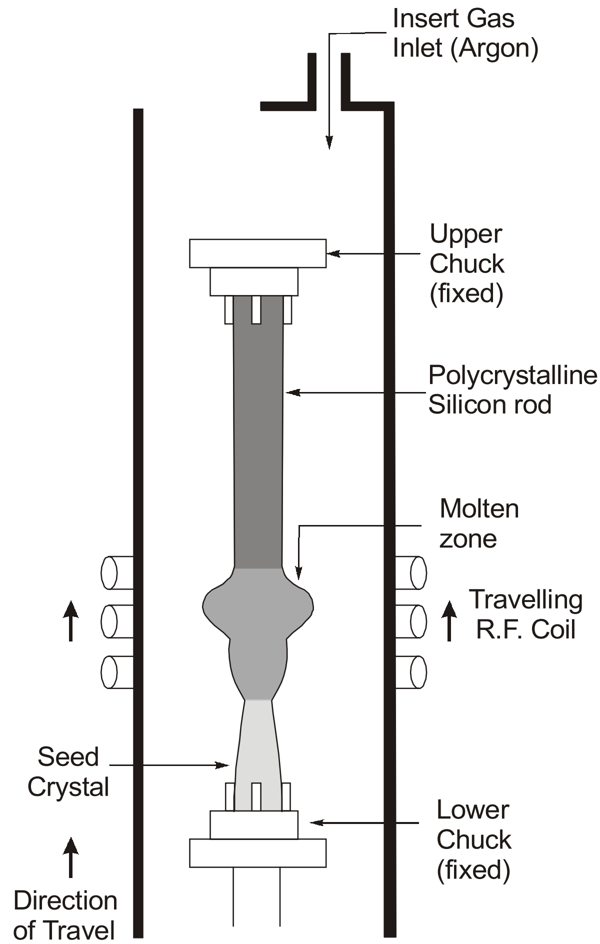
To grow a SiO_2 layer of 100 nm, the thickness of Si consumed will be,

$$\text{Thickness of Si} = (0.44)\,(100) = 44\text{ nm}$$

Q.5 Explain briefly the float-zone crystal growth process with a neat diagram.

Solution:

The float-zone process can be used to grow silicon that has lower contaminations than that normally obtained from the Czochralski technique. A schematic setup of the float zone process is shown in the figure.



A high purity polycrystalline rod with a seed crystal at the bottom is held in a vertical position and rotated. The rod is enclosed in a quartz envelope within which an inert atmosphere (argon) is maintained.

During the operation, a small zone (a few centimeters in length) of the crystal is kept molten by a radio-frequency heater, which is moved from the seed upward so that this floating zone traverses the length of the rod. The molten silicon is retained by surface tension between the melting and growing solid-silicon faces. As the floating zone moves upward, a single-crystal silicon freezes at the zone's retreating end and grows as an extension of the seed crystal and the solidified region has the same orientation as the seed.

Materials with higher resistivities can be obtained from the float-zone process than from the Czochralski process because it can be used to purify the crystal more easily. The furnace is filled with an inert gas like argon to reduce gaseous impurities. Also, since no crucible is needed, it can be used to produce oxygen 'free' Si wafers.

At the present time, float-zone crystals are used mainly for high-power, high-voltage devices, where high-resistivity materials are required.

The difficulty is to extend this technique for large wafers, since the process produces large number of dislocations.

Q.6 Explain briefly the following process techniques involved in IC fabrication:

(i) Diffusion (ii) Ion implantation

Solution:

(i) Diffusion: Diffusion is the movement of impurity atoms in a semiconductor material at high temperatures. The driving force of diffusion is the concentration gradient. There is a wide range of diffusivities for various dopant species, which depend on how easy the respective dopant impurity can move through the material. Diffusion is applied to anneal the crystal defects after ion implantation or to introduce dopant atoms into silicon from a chemical vapour source. In the lateral case the diffusion time and temperature determine the depth of dopant penetration. But diffusion can also be an unwanted parasitic effect, because it takes place during all high temperature process steps.

The biggest limitation of thermal diffusion is that the process is isotropic, i.e. lateral diffusion cannot be avoided, though diffusion coefficients in different crystallographic directions might be different. Thus, an oxide window that serves as a mask to protect certain regions of the wafers can be ineffective due to lateral diffusion. This is especially important for doping small regions. Doping control is also difficult to achieve due to presence of concentration gradients. These gradients will change in subsequent annealing steps. Thus, there is a thermal budget associated with doping.